SPECIFICATION

[Title of the Invention]

Ferroelectric memory device and fabrication method therefor

[Brief Description of the Drawings]

FIG. 1 is a sectional view of a FRAM device according to a first embodiment of the present invention, in which a method for detecting a charge change in the ferroelectric capacitor is adopted;

FIG. 2 is a sectional view of a FRAM device according to a second embodiment of the present invention, in which a method for detecting a charge change in the ferroelectric capacitor is adopted;

FIG. 3 is a sectional view of a FRAM device according to a third embodiment of the present invention, in which a method for detecting a resistance changes of a semiconductor due to spontaneous polarization of a ferroelectric material;

FIG. 4 is a sectional view of a FRAM device according to a fourth embodiment of the present invention, in which a method for detecting a resistance changes of a semiconductor due to spontaneous polarization of a ferroelectric material; and

FIGs. 5 through 7 are sectional views of intermediate structures for illustrating a fabrication method of a FRAM device according to a first embodiment of the present invention, shown in FIG. 1.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a semiconductor memory device and a fabrication method therefor, and more particularly, to a ferroelectric random access memory (FRAM) device and a fabrication method therefor.

A ferroelectric material has a ferroelectricity. The ferroelectricity is a physical

property in which if an external voltage is applied to electric dipoles arranged in the ferroelectric material, a spontaneous polarization of the electric dipoles is generated, and remanent polarization of a constant level remains even after the external electric field is removed. When the remanent polarization of the ferroelectric material is used for storing data, the data can be stored without an external voltage. Also, reversal of the external field causes polarization in the opposite direction.

The FRAMs using the ferroelectric material are largely classified into two types; a method for detecting a change in charge amount stored in a ferroelectric capacitor, and a method for detecting a change in resistances of a semiconductor due to spontaneous polarization of the ferroelectric material.

The method for detecting a charge change in the ferroelectric capacitor is typically adapted to a structure in which a unit cell is constituted by one capacitor and one transistor. Particularly, this method is widely applied to a DRAM, such that a thick interlayer insulating layer is formed on a CMOS structure and a ferroelectric capacitor is formed thereon.

The method for detecting a resistance changes of a semiconductor due to spontaneous polarization of a ferroelectric material is typically adapted to a metal ferroelectric metal insulator semiconductor (MFMIS) field effect transistor (FET) structure. In the MFMIS FET structure, a unit cell is constituted by one transistor.

Both methods have a ferroelectric capacitor structure formed by depositing a lower metal layer/a ferrorelectric layer/a upper metal layer.

The most widely used ferroelectric capacitor is a ferroelectric layer using PZT ($Pb(Zr_xTi_{1-x})O_3$). The PZT ($Pb(Zr_xTi_{1-x})O_3$) is used because its Curie temperature is relatively high, i.e., 230~490°C, has a different crystalline phases according to Zr/Ti composition and temperature and a high dielectric constant.

However, in the conventional capacitor having a structure of lower metal layer-PZT layer-upper metal layer, an imprint phenomenon in which a hysteresis curve moves toward a positive or negative direction along an electric field axis occurs. If the imprint phenomenon occurs, the absolute values of positive and negative coercive

voltages become different from each other, which destroys symmetry and reduces a remnant polarization value Pr.

The imprint phenomenon is caused by a in characteristics difference between an upper interface between the upper metal layer and PZT layer and a lower interface between lower metal layer and PZT layer. The characteristics difference is caused by a thermal treatment of the PZT layer. In other words, after the PZT layer is deposited on the lower metal layer, if the PZT layer is thermally treated for crystallization, Pb present in the PZT layer moves toward the interface adjacent the lower metal layer to change the interface characteristics. However, since the upper metal layer is formed on the thermally treated PZT layer, is does not experience such a change as the lower metal layer. Thus, the upper and lower interfaces of the PZT layer become different in their characteristics, causing the imprint phenomenon.

[Technical Goal of the Invention]

To solve the above problems, it is an object of the present invention to provide a ferroelectric random access memory (FRAM) device having a ferroelectric layer with the same characteristics of upper and lower interfaces so that an imprint phenomenon does not occur.

It is another object of the present invention to provide a fabrication method suitable for fabricating a FRAM device having a ferroelectric layer with the same upper and lower interface characteristics.

[Structure and Operation of the Invention]

According to an aspect of the present invention, there is provided a FRAM device having a ferroelectric capacitor including seed layers above and below a ferroelectric layer. The FRAM device according to the present invention has a ferroelectric capacitor including a lower electrode, a lower seed layer, a ferroelectric layer, an upper seed layer, and an upper electrode, which are sequentially layered on a semiconductor substrate.

According to another aspect of the present invention, there is provided a method for fabricating a FRAM device, comprising sequentially forming a lower electrode, a lower seed layer, a ferroelectric layer, and an upper seed layer on a semiconductor substrate, thermally treating the resultant structure having the upper seed layer to make the characteristics of lower and upper faces of the ferroelectric layer be the same with each other and to complete a stable perovskite crystal structure of the ferroelectric layer, and then forming an upper electrode.

In an embodiment of the present invention, the ferroelectric layer may be formed of PZT. The upper and lower seed layers may be formed of a material capable of making the characteristics of the upper and lower interfaces of the ferroelectric layer be the same with each other, for example, a material having a crystallization temperature lower than that of a material for forming the ferroelectric layer or a ferroelectric material having a lattice constant similar to that of a material for forming the ferroelectric layer. Thus, $PbTiO_3$, TiO_3 or PZT having a more Pb content and a higher Ti/Zr ratio than a PZT to be used to form the ferroelectric layer may be used.

The lower electrode may be formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer, and the upper electrode may be formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer.

According to the present invention, since the characteristics of the upper and lower interfaces become the same with each other by upper and lower seed layers, an imprint phenomenon can be effectively prevented in the ferroelectric random access memory device having a lower seed layer-ferroelectric layer-upper seed layer structure.

The present invention will be described in detail through preferred embodiments with reference to accompanying drawings. However, the present invention is not limited to the following embodiments but may be implemented in various types. The preferred embodiments are only provided to make the disclosure of the invention perfect and make one having an ordinary skill in the art know the scope of the invention. The thicknesses of various layers and regions are emphasized for clarity in accompanying

drawings. Also, when a layer is defined to exist on another layer or a substrate, the layer may exist directly on another layer or substrate, or an interlayer layer may be present therebetween. Throughout the drawings, the same reference numerals denote the same elements.

<Ferroelectric random access memory device>

FIRST EMBODIMENT

FIG. 1 is a sectional view of a FRAM device according to a first embodiment of the present invention, in which a method for detecting a charge change in the ferroelectric capacitor is adopted.

A transistor comprised of a gate 104 formed by interposing a gate insulating layer 102 on a semiconductor substrate 100, a source region 106 and a drain region 107, is formed. An interlayer insulating film 108 comprised of one selected from phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), tetraethyl orthosilicate (TEOS) and unhoped silicate glass (USG) is deposited on the entire surface of the substrate 100 in which the transistor is formed. A contact plug 110 formed in the interlayer insulating film is in contact with the source region 106 of the transistor. A lower electrode 112 is formed on the contact plug 110. A dielectric layer D comprised of a lower seed layer 114, a ferroelectric layer 116 and an upper seed layer 118 is deposited on the lower electrode 112, and an upper electrode 120 is formed on the upper seed layer 118, to thus complete a ferroelectric capacitor.

The seed layers 114 and 118 formed above and below the ferroelectric layer 116 prevent an imprint phenomenon from being generated in a ferroelectric capacitor by making the characteristics of the upper and lower interfaces of the ferroelectric layer same with each other. The upper and lower seed layers 114 and 118 of the ferroelectric layer 116 are preferably formed of a material having a low crystallization temperature. This is because it is possible to make the characteristics of the upper and lower interfaces be the same with each other, by crystallizing the upper and lower seed layers 114 and 118 prior to the ferroelectric layer 116 during a thermal treatment

for crystallizing the ferroelectric layer 116 into a stable perovskite structure, and thus the ferroelectric layer 116 is crystallized from the upper and lower faces toward the center thereof. The upper and lower seed layers 114 and 118 are more preferably formed of a material having a ferroelectricity, i.e., having a lattice constant similar to that of the ferroelectric layer 116.

For example, in the case of forming the ferroelectric layer 116 using PZT, the upper and lower seed layers 114 and 118 are preferably formed using $PbTiO_3$ or TiO_2. Also, PZT having a rich Pb content and a higher Ti composition ratio may be used, compared to the PZT forming the ferroelectric layer 116. If the contents of Pb exceeds 120% based on other constituents, or the value of Ti/Zr is greater than 48/52, that is to say, the Ti composition ratio is high, crystallization occurs well. Therefore, the seed layers 114 and 118 formed above and below the PZT layer 116 are first crystallized compared to the PZT layer 116 during the thermal treatment of the PZT layer 116. Thus, the PZT layer is crystallized toward the center from above and below faces thereof. Also, elements such as Pb is prevented from being diffused out to the upper and lower electrodes. Therefore, the upper and lower interfaces of the PZT layer are formed to have the same characteristics.

It is preferable that the upper and lower electrodes 120 and 112 each is formed of a material having a high barrier characteristics at the interfaces from the ferroelectric layer 16 and a stable material which is not reactive with a ferroelectric material. Therefore, a Pt-group metal such as Pt, Ir, Ru or Rh is used as an electrode material. The upper and lower electrodes 120 and 112 are also formed of a conductive oxide such as IrO_2, RuO_2, RhO_2 or $LaSrCoO_3$, improving fatigue characteristics.

SECOND EMBODIMENT

FIG. 2 is a sectional view of a FRAM device according to a second embodiment of the present invention, in which a method for detecting a charge change in the ferroelectric capacitor is adopted. The FRAM device according to the second embodiment of the present invention is different from that according to the first

embodiment of the present invention in that a lower electrode is comprised of a dual layer of a Pt-group metal layer 112 and a conductive oxide layer 113, and an upper electrode is comprised of a dual layer of a conductive oxide layer 119 and a Pt-group metal layer 120. The conductive oxide layers 113 and 119 are further formed as the constituents of the upper and lower electrodes because fatigue may be generated at a capacitor if the upper and lower electrodes thereof are formed of only Pt-group metal layers. Therefore, each conductive oxide layer is further formed between the upper seed layer and the upper Pt-group metal layer, and between the lower seed layer and the lower Pt-group metal layer, thereby improving the fatigue characteristics. The finally obtained capacitor is comprised of a lower Pt-group metal layer-lower conductive oxide layer-lower seed layer-ferroelectric layer-upper seed layer-upper conductive oxide layer-upper Pt-groups metal layer, and the respective layers are symmetric in view of the ferroelectric layer in the middle of the entire structure. Thus, according to the second embodiment of the present invention, an imprint phenomenon is prevented from being generated in the ferroelectric capacitor.

As a material for forming the conductive oxide layers 113 and 119, IrO_2, RuO_2, RhO_2 or $LaSrCoO_3$ is preferably used.

THIRD EMBODIMENT

FIG. 3 is a sectional view of a FRAM device according to a third embodiment of the present invention, in which a method for detecting a resistance changes of a semiconductor due to spontaneous polarization of a ferroelectric material.

A gate insulating layer 303 is formed on a semiconductor substrate 300, and a lower electrode 304, a lower seed layer 306, a ferroelectric layer 308, an upper seed layer 310 and an upper electrode 312 are sequentially formed on the gate insulating layer 303. Also, source and drain regions 301 and 302 are formed in the semiconductor substrate 300 adjacent to the periphery of the gate insulating layer 303. Generally, the source and drain regions 301 and 302 are formed after the upper electrode 312 is formed.

In the FRAM device shown in FIG. 3, the on/off state of a channel which is to be induced in the semiconductor substrate 300 being under the gate insulating layer 303 is determined by the direction of a polarity of the ferroelectric capacitor. For example, if the channel is turned on, data is read as '1', and if the channel is turned off, data is read as '0'.

The FRAM device according to the third embodiment of the present invention is different from that according to the first embodiment of the present invention in that a memory cell is formed of one transistor. In contrast therewith, the FRAM device according to the first embodiment of the present invention is comprised of a transistor and a capacitor. However, those are the same with each other in that both FRAM devices employ a capacitor having a structure of lower electrode-lower seed layer-ferroelectric layer-upper seed layer-upper electrode. Thus, the explanation of the respective constituents will be omitted herein.

FOURTH EMBODIMENT

FIG. 4 is a sectional view of FRAM device according to a fourth embodiment of the present invention, in which a method for detecting a resistance changes of a semiconductor due to spontaneous polarization of a ferroelectric material.

With the exception of conductive oxide layers 305 and 311 being further provided between the upper/lower seed layers 306/310 and the upper/lower electrodes 304/312, this embodiment is the same as the third embodiment. The reason of forming the conductive oxide layers 305 and 311 is as described in the second embodiment.

<Fabrication method of FRAM device>

The fabrication method of the FRAM device according to the first embodiment of the present invention will be described with reference to FIGS. 5 through 7.

Referring to FIG. 5, a transistor comprised of a gate insulating layer 102, a gate electrode 104, a source region 106 and a drain region 107 is formed on a semiconductor substrate 100 in a conventional manner. Subsequently, an insulating

material selected from PSG, BPSG, TEOS and USG is deposited on the entire surface of the resultant structure and planarized to form an interlayer insulating film 108. Next, the interlayer insulating film 108 is partly etched to form a contact hole exposing the source region 106 and the contact hole is filled with a conductive material, thereby forming a conductive plug 110 connecting a source of the transistor and a lower electrode of the capacitor.

Then, a material for forming the lower electrode of the capacitor is deposited on the resultant structure in which the conductive plug 112 is formed, and then patterned using a conventional photolithography to form a lower electrode 112 of the capacitor. Here, the lower electrode of the capacitor is formed of a Pt-group metal such as Pt, Ir, Ru or Rh, a conductive oxide such as IrO_2, RuO_2, RhO_2 or $LaSrCoO_3$, or a dual layer of a Pt-group metal layer and a conductive oxide layer.

Referring to FIG. 6, a lower seed layer 114, a ferroelectric layer 116 and an upper seed layer 118 are sequentially formed on the entire surface of the resultant structure in which the lower electrode 112 is formed. After the layers including the upper seed layer 118 are formed, the resultant structure is thermally treated, thereby crystallize a perovskite structure of the ferroelectric layer 116 and stabilizing the same.

Here, the lower seed layer 114 and the upper seed layer 118 must be formed of a material which induces the ferroelectric layer 116 to be crystallized into an uniform and stable perovskite structure throughout the ferroelectric layer during a thermal treatment so that the characteristics of the upper and lower interfaces of the ferroelectric layer 116 are made to be the same with each other. Therefore, the lower seed layer 114 and the upper seed layer 118 must be formed of a material having a lower crystallization temperature than that of the ferroelectric layer 116. Also, the lower seed layer 114 and the upper seed layer 118 must be formed of a material having a lattice constant similar to that of the ferroelectric layer 116. The reason of the foregoing is as follows. If the lower seed layer 114 and the upper seed layer 118 are crystallized prior to the ferroelectric layer 116 during the thermal treatment, since crystallization occurs from the upper and lower faces to the center of the ferroelectric layer 116, the upper

and lower interfaces of the ferroelectric layer 116 are formed to be the same with each other. Also, the seed layers 114 and 118 are more preferably formed of a material having a ferroelectricity in consideration of a capacitance of the capacitor.

Therefore, if the ferroelectric layer 116 is formed of PZT, the seed layers 114 and 118 are more preferably formed using $PbTiO_3$, TiO_2 or PZT having a rich Pb content and a higher Ti composition ratio, compared to the PZT forming the ferroelectric layer 116. For example, if the contents of Pb exceeds 120% based on other constituents, or the value of Ti/Zr is greater than 48/52, that is to say, the Ti composition ratio is high, crystallization occurs well.

In the case of forming the lower seed layer 114 using $PbTiO_3$, a sputtering method, a metal organic chemical vapor deposition (MOCVD) method or a sol-gel method may be employed.

In the case of using the MOCVD method, as a CVD source, tetra-ethyl lead or titanium isopropoxide may be used.

In the case of using the sol-gel method, a mixed solution of lead acetate and titinium isopropoxide is deposited on the semiconductor substrate 100 by a rotation coating process, and thermally treated in the range of 500~700°C.

The lower seed layer 114 is preferably formed to a thickness of below 200Å .

The ferroelectric layer 116 is formed of a sputtering method, a MOCVD method or a sol-gel method. The ferroelectric layer 116 is formed of an oxide having a perovskite structure, e.g., PZT.

In the case of depositing the PZT layer by the sputtering method, while the temperature of a substrate is set to 450~650° C and the chamber pressure is maintained as 1~10 mTorr, a PZT target, e.g., a target having a composition of $Pb(Zr_{0.6}Ti_{0.4})O_3$ and PbO(20 mol %) is sputtered under an atmosphere containing argon (Ar) and oxygen (O_2) to form the PZT layer. Also, in the case of depositing the PZT layer by the CVD method, tetra-ethyl lead, titanium isopropoxide and zirconium n-butoxide are used as the main components of the CVD source. An oxidizing gas, i.e., a source gas containing 10~50% N_2O and O_2, is flowed, with Ar as a carry gas, to a

chamber in which the substrate temperature is set to 450~650° C and the chamber pressure is maintained as 0.1~10 Torr.

The upper seed layer 118 is formed in the same manner as the lower seed layer 114.

Referring to FIG. 7, the upper electrode 120 is formed on the upper seed layer 118 using the same material with that of the lower electrode 112, for the purpose of making the upper and lower components symmetric with each other based on the ferroelectric layer 116. This helps preventing an imprint phenomenon, i.e., making the characteristics of the upper and lower interfaces of the ferroelectric layer 116 be the same with each other.

Finally, the upper electrode 120, the upper seed layer 118, the ferroelectric layer 116 and the lower seed layer 114 are patterned to units of cells by a conventional photolithography, thereby completing a capacitor cell unit.

The present invention has been illustrated and described with reference to specific embodiments and specific terms have been used throughout the drawings and detailed description of the invention, which is not intended limiting the scope of the invention as claimed in the appended claims but is just adopted for technical concepts. Therefore, it should be understood that the invention is not limited to the illustrated embodiment and that many changes and modifications can be made within the scope of the invention by a person skilled in the art.

[Effect of the Invention]

The FRAM device according to the present invention includes seed layers above and below a ferroelectric layer. The seed layers formed above and below faces of the ferroelectric layer can prevent an imprint phenomenon from being generated in a ferroelectric capacitor by making the characteristics of the upper and lower interfaces of the ferroelectric layer be the same with each other. In other words, the upper and lower seed layers are crystallized prior to the ferroelectric layer from the upper and lower faces of the ferroelectric layer toward the center thereof during a thermal

treatment. Therefore, the characteristics of the upper and lower interfaces of the ferroelectric layer are made to be the same with each other, thereby improving ferroelectric capacitor characteristics.